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ANALYSIS AND OPTIMIZATION DESIGN OF SIGNAL INTEGRITY IN OPTOELECTRONIC INTEGRATED SYSTEMS

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Abstract: With the rapid development of high-speed communications, artificial intelligence computing, data centers, and advanced packaging technologies, optoelectronic integrated systems have shown great potential for high-bandwidth, low-power, and high-density interconnect applications. However, in practical systems, high-speed electrical signals still propagate through packaging interconnects, differential transmission lines, pads, vias, and electro-optic modulator interfaces, where they are susceptible to impedance discontinuity, insertion loss, signal reflection, crosstalk, and bandwidth limitation. These impairments can degrade the electrical eye diagram and further reduce the optical modulation quality. This paper investigates signal integrity issues in optoelectronic integrated systems by analyzing the main degradation mechanisms along the high-speed electrical interconnect path and at the electro-optic conversion interface. Optimization strategies are discussed from the perspectives of impedance matching, interconnect structure optimization, crosstalk suppression, and driver–modulator co-design. The results indicate that system-level signal integrity optimization can effectively reduce high-frequency loss and reflection, improve eye opening, and enhance the effective driving voltage at the modulator input as well as the optical output quality. This work provides useful guidance for the design of high-bandwidth, low-power, and highly reliable optoelectronic integrated systems.
Keywords: Optoelectronic integrated systems; Signal integrity; Interconnect structure optimization; Driver–modulator co-design

1 INTRODUCTION

With the rapid development of high-speed communications, data centers, artificial intelligence computing, and advanced packaging technologies, electronic systems are facing increasingly stringent requirements for data rate, bandwidth density, and energy efficiency[1-2]. Conventional electrical interconnects suffer from conductor loss, dielectric loss, impedance discontinuity, enhanced crosstalk, and increased power consumption under high-frequency and high-speed operating conditions, which have gradually become major bottlenecks limiting further system performance improvement[3-4]. Optoelectronic integrated systems, which combine electronic integrated circuits with photonic integrated devices, provide a promising technical approach for next-generation high-speed interconnects and high-performance computing systems by exploiting the advantages of optical signals in high-speed transmission, low loss, and large bandwidth. However, in practical optoelectronic integrated systems, high-speed electrical signals still need to propagate through drivers, packaging interconnects, transmission lines, pads, vias, and electro-optic modulator interfaces. The quality of these electrical signals directly affects the subsequent optical modulation process and the overall transmission reliability of the system. Therefore, signal integrity analysis and optimization design for optoelectronic integrated systems are of great significance.

At present, signal integrity analysis for high-speed electronic systems has been extensively investigated, with established methods mainly focusing on impedance matching, S-parameter analysis, eye diagram evaluation, crosstalk suppression, and high-speed interconnect optimization. Meanwhile, with the development of silicon photonics, co-packaged optics, and heterogeneous optoelectronic integration, increasing attention has been paid to high-speed interconnections between electronic chips and photonic chips. Nevertheless, existing studies often focus on individual electrical interconnect structures, packaging channels, or photonic device characteristics, while the coupled effects among high-speed electrical interconnects, packaging parasitics, and electro-optic conversion interfaces in optoelectronic integrated systems remain insufficiently addressed. In particular, under high-density, multi-channel, and high-speed modulation conditions, impedance discontinuity, insertion loss, signal reflection, crosstalk, and input mismatch at the modulator interface can jointly degrade both the electrical eye diagram and the optical output quality[5-6]. Therefore, a system-level analysis of signal integrity issues in optoelectronic integrated systems is necessary, together with optimization strategies suitable for practical engineering design[7-8].

In this paper, the signal integrity issues in optoelectronic integrated systems are investigated, with particular emphasis on the degradation mechanisms of high-speed signals along the electrical interconnect path and at the electro-optic conversion interface. First, the effects of impedance discontinuity, signal reflection, insertion loss, bandwidth limitation, inter-symbol interference, and crosstalk on system transmission performance are analyzed. Then, considering the structural characteristics of optoelectronic integrated systems, the interface matching between the driver and the modulator is discussed, together with its influence on optical modulation quality. Finally, signal integrity optimization strategies are proposed from the perspectives of impedance matching, interconnect structure optimization, crosstalk suppression, and driver–modulator co-design. This work aims to establish a concise and effective analysis and

optimization framework, providing a useful reference for the design of high-bandwidth, low-power, and highly reliable optoelectronic integrated systems.

2 SIGNAL INTEGRITY ISSUES IN OPTOELECTRONIC INTEGRATED SYSTEMS

In optoelectronic integrated systems, the high-speed signal path usually consists of multiple components, including electronic chips, packaging interconnects, transmission lines, pads, vias, and electro-optic modulators. Compared with conventional electrical interconnect systems, optoelectronic integrated systems require not only the evaluation of electrical signal transmission quality, but also the consideration of how electrical signal degradation affects the optical modulation process. Therefore, signal integrity is no longer limited to a single electrical channel. Instead, it becomes a coupled problem involving electrical interconnects, packaging structures, and electro-optic conversion interfaces. This section analyzes the main signal integrity issues from three aspects: impedance discontinuity and signal reflection, insertion loss and bandwidth limitation, and crosstalk together with electro-optic interface coupling.

2.1 Impedance Discontinuity and Signal Reflection

Impedance continuity is one of the key factors affecting high-speed signal transmission quality. In optoelectronic integrated systems, high-speed signals are typically delivered from the driver output through packaging substrates, interposers, differential transmission lines, pads, and vias before reaching the input terminal of the electro-optic modulator. Since different regions may have different dielectric constants, geometrical dimensions, reference planes, and connection structures, local impedance discontinuities can easily occur along the signal path.

When a high-speed signal encounters an impedance discontinuity, part of the signal energy is reflected, leading to degraded return loss. In the time domain, signal reflection is usually observed as overshoot, ringing, and waveform distortion, which further increase jitter and reduce the eye opening. For high-speed differential signals, impedance discontinuity may also disturb differential symmetry, introduce common-mode noise and mode conversion, and reduce the noise immunity of the link.

In optoelectronic integrated systems, impedance matching between the driver and the modulator is particularly important. The input of an electro-optic modulator usually includes parasitic capacitance, electrode resistance, and frequency-dependent impedance characteristics, and therefore cannot be simply treated as an ideal load. If the driver output impedance, the characteristic impedance of the transmission line, and the modulator input impedance are not properly matched, reflected signals may accumulate along the channel, causing distortion of the effective driving voltage at the modulator input. This distortion can further degrade the quality of optical modulation. Therefore, signal integrity analysis in optoelectronic integrated systems should pay close attention to impedance discontinuities introduced by transmission lines, pads, vias, packaging interconnects, and the modulator input interface.

2.2 Insertion Loss, Bandwidth Limitation, and Inter-Symbol Interference

As the signal data rate and operating frequency increase, insertion loss in high-speed interconnect channels becomes more significant. Insertion loss mainly originates from conductor loss, dielectric loss, skin effect, packaging parasitics, and electrode loss in electro-optic modulators. At high frequencies, the transmission channel attenuates high-frequency components more strongly, resulting in slower rising and falling edges and a reduced effective bandwidth.

Bandwidth limitation leads to inter-symbol interference. When waveforms of adjacent symbols overlap with each other, the receiver or the modulator input becomes less capable of distinguishing different logic states, resulting in eye closure and an increased bit error rate. For NRZ signals, inter-symbol interference is mainly reflected in reduced eye height and eye width. For multi-level modulation formats such as PAM4, the impact of insertion loss and inter-symbol interference becomes more severe because the voltage spacing between adjacent levels is smaller.

In optoelectronic integrated systems, the insertion loss of the electrical interconnect channel not only affects the electrical signal itself, but also influences the electro-optic conversion process. If the voltage swing arriving at the modulator input is insufficient, the modulator cannot be driven effectively, leading to reduced optical modulation amplitude, degraded extinction ratio, and deterioration of the optical eye diagram. Therefore, insertion loss and bandwidth limitation should be evaluated from both the electrical transmission perspective and the optical modulation perspective. In other words, signal integrity analysis in optoelectronic integrated systems should consider not only whether the electrical eye diagram remains open, but also whether the degraded electrical signal leads to reduced optical output performance.

2.3 Crosstalk and Electro-Optic Interface Coupling

Optoelectronic integrated systems are usually characterized by high-density and multi-channel architectures, such as multi-channel optical transceivers, silicon photonic arrays, and co-packaged optical systems. To increase bandwidth density, multiple high-speed channels are often arranged within a limited chip or package area. When the spacing between adjacent signal lines is small, the parallel coupling length is long, or the reference plane is discontinuous, electromagnetic coupling becomes stronger and crosstalk is generated.

Crosstalk mainly includes near-end crosstalk and far-end crosstalk. Near-end crosstalk introduces interference near the transmitting side, while far-end crosstalk propagates toward the receiving side or the modulator input and appears as

superimposed noise on the desired signal. Crosstalk increases eye diagram noise, aggravates jitter, and reduces the voltage margin for signal decision. In multi-channel PAM4 or higher-speed optoelectronic systems, the influence of crosstalk on system reliability becomes more critical because multi-level signals inherently have smaller noise margins.

In addition to channel-to-channel crosstalk, electro-optic interface coupling is another important issue unique to optoelectronic integrated systems. The electro-optic modulator acts both as an electrical load and as the core device for optical signal modulation. Its input capacitance, input impedance, electrode loss, bias condition, and modulation efficiency all affect the conversion from electrical signals to optical signals. When impedance or bandwidth mismatch exists between the driver and the modulator, insufficient voltage swing, waveform distortion, and modulation nonlinearity may still occur at the modulator input, even if the preceding electrical channel exhibits acceptable transmission performance.

Therefore, signal integrity issues in optoelectronic integrated systems exhibit strong system-level coupling characteristics. Impedance discontinuity, insertion loss, reflection, and crosstalk first degrade the electrical signal quality and subsequently affect the effective driving voltage, optical modulation amplitude, extinction ratio, and optical eye diagram of the modulator. Compared with conventional high-speed electrical interconnect systems, signal integrity analysis for optoelectronic integrated systems must consider both electrical transmission characteristics and electro-optic conversion performance, which forms the basis for the following optimization design.

3 OPTIMIZATION DESIGN OF SIGNAL INTEGRITY

To address impedance discontinuity, insertion loss, crosstalk, and electro-optic interface mismatch in optoelectronic integrated systems, signal integrity optimization should be performed from a system-level perspective. Compared with conventional high-speed electrical interconnect systems, the optimization objective in optoelectronic integrated systems is not only to improve the transmission quality of electrical signals, but also to ensure that the electrical signals can effectively drive the electro-optic modulator and generate stable optical modulation output. Therefore, this section focuses on three major aspects: impedance matching and interconnect structure optimization, crosstalk suppression in high-density channels, and driver–modulator co-design.

3.1 Impedance Matching and Interconnect Structure Optimization

Impedance matching is fundamental to improving high-speed signal transmission quality. In optoelectronic integrated systems, high-speed signals propagate from the driver output to the input of the electro-optic modulator through packaging substrates, differential transmission lines, pads, vias, interposers, and chip-to-chip interconnects. Variations in geometry, material properties, and reference planes in these structures may introduce impedance discontinuities, resulting in signal reflection and waveform distortion. Therefore, the primary goal of interconnect structure optimization is to improve impedance continuity along the signal path.

For high-speed differential interconnect channels, the transmission line width, spacing, dielectric thickness, and reference ground structure should be properly designed so that the differential impedance remains close to the target value. In general, a stable characteristic impedance is required for high-speed differential channels to reduce reflection and improve transmission efficiency. Meanwhile, the layout of transmission lines should be kept as symmetric as possible, avoiding sharp bends and unnecessary length mismatch, so as to reduce mode conversion and differential imbalance.

Local interconnect structures such as pads, vias, and BGA solder balls are important sources of high-frequency discontinuities. Vias introduce parasitic inductance and capacitance, while via stubs may cause resonances and increase high-frequency insertion loss. To mitigate these effects, methods such as reducing via stubs, optimizing anti-pad dimensions, adding ground via shielding, shortening the signal path, and maintaining reference plane continuity can be adopted to improve transmission performance. For the high-speed connection between the driver and the modulator, the path length and parasitic parameters should be minimized to ensure that the electrical signal reaches the modulator input with reduced loss and reflection.

Therefore, impedance matching and interconnect structure optimization should not be regarded as the adjustment of a single structural parameter. Instead, the key objective is to maintain impedance continuity and stable electromagnetic field distribution throughout the entire high-speed signal path. By reducing local discontinuities, lowering high-frequency loss, and improving the return current path, the signal integrity of the system can be effectively enhanced, providing more stable driving conditions for subsequent electro-optic conversion.

3.2 Crosstalk Suppression in High-Density Channels

As optoelectronic integrated systems evolve toward higher bandwidth density and multi-channel parallel transmission, crosstalk suppression becomes a critical issue in signal integrity optimization. Within limited chip and package areas, multiple high-speed differential channels are often placed in close proximity. If the spacing between adjacent channels is too small, the parallel routing length is too long, or the reference plane is improperly designed, electromagnetic coupling between channels becomes stronger, leading to increased near-end and far-end crosstalk.

Crosstalk is superimposed on the desired signal as noise, increasing eye diagram noise, aggravating jitter, and reducing the signal decision margin. For multi-level modulation formats such as PAM4, the impact of crosstalk on system performance becomes more pronounced because the voltage spacing between adjacent levels is relatively small.

Therefore, in high-density optoelectronic integrated systems, a careful trade-off between channel density and signal integrity is required.

Crosstalk can be reduced through layout optimization, shielding, and reference plane improvement. First, the spacing between adjacent channels should be properly controlled, and long parallel routing sections should be minimized to avoid strong coupling regions. Second, ground traces or ground vias can be introduced near critical signal channels to provide effective electromagnetic shielding and reduce channel-to-channel coupling. Third, the continuity and integrity of the reference plane should be maintained to prevent additional noise coupling caused by discontinuous return current paths.

In addition, channel arrangement in multi-channel systems also affects the crosstalk level. For high-density differential channels, crosstalk can be further suppressed by optimizing the routing order, adjusting the direction of adjacent channels, adopting symmetric layouts, and isolating sensitive signals. In practical designs, simply increasing channel spacing can effectively reduce crosstalk, but it sacrifices system integration density. Therefore, a more reasonable approach is to combine shielding structures, reference plane optimization, and channel layout design within a limited area, achieving a balance between bandwidth density and signal integrity.

3.3 Driver–Modulator Co-Design

The driver–modulator interface is one of the most representative electro-optic coupling sections in optoelectronic integrated systems, and it is also the key aspect that distinguishes signal integrity optimization in optoelectronic systems from that in conventional high-speed electrical interconnects. In traditional electrical interconnect systems, the optimization objective is usually to obtain a high-quality electrical eye diagram at the receiver. In optoelectronic integrated systems, however, the objective also includes ensuring that the electro-optic modulator receives a sufficient and stable driving signal to generate high-quality optical output.

An electro-optic modulator is not an ideal electrical load. Its input terminal usually includes junction capacitance, electrode resistance, parasitic inductance, and frequency-dependent impedance characteristics. When the driver output impedance, interconnect characteristic impedance, and modulator input impedance are not well matched, reflection and high-frequency attenuation occur, reducing the effective driving voltage at the modulator input. Meanwhile, the modulation bandwidth and modulation efficiency of the modulator also limit the conversion quality from electrical signals to optical signals, leading to reduced optical modulation amplitude, degraded extinction ratio, and deterioration of the optical eye diagram.

Therefore, driver–modulator co-design should simultaneously consider electrical signal transmission performance and optical modulation performance. On the driver side, the output impedance, voltage swing, and pre-emphasis capability should be properly designed so that the driver can compensate for high-frequency loss in the interconnect channel. On the modulator side, the input capacitance, electrode structure, bias point, and termination scheme should be optimized to improve bandwidth and reduce reflection. At the interface level, good impedance matching among the driver, interconnect channel, and modulator should be maintained, ensuring a stable effective driving voltage at the modulator input.

Moreover, driver–modulator co-design should also consider the trade-off between power consumption and performance. Increasing the driving voltage swing can improve optical modulation amplitude, but it also increases driver power consumption and may introduce stronger nonlinear distortion. Reducing the modulator capacitance can improve bandwidth, but it may be constrained by device structure and fabrication processes. Therefore, practical optimization should comprehensively consider electrical eye quality, optical modulation amplitude, extinction ratio, bit error rate, and power consumption.

In summary, signal integrity optimization in optoelectronic integrated systems should be extended from pure electrical channel optimization to electro-optic interface co-design. Only by simultaneously improving the high-speed interconnect path and the driver–modulator interface can the quality of electrical signals be effectively converted into optical signal quality, thereby enhancing the transmission performance and reliability of the entire optoelectronic integrated system.

4 RESULTS AND DISCUSSION

4.1 Simulation Setup

A representative 112 Gb/s PAM4 optoelectronic integrated interconnect was modeled to investigate the electrical-optical signal transmission across heterogeneous platforms. As shown in Figure 1, the system consists of a PRBS/PAM4 source and electrical driver, a package substrate or interposer carrying differential transmission lines with via transitions and pad interfaces, and an electro-optic modulator that converts the electrical PAM4 signal into the optical domain. The optical output is coupled to an on-chip waveguide for downstream delivery.

To comprehensively evaluate system behavior, both frequency-domain and time-domain co-simulations were performed. S-parameter analysis was used to quantify the influence of impedance discontinuity, insertion loss, and crosstalk over a broad frequency range, while transient simulations were employed to assess the impact on waveform integrity and optical modulation quality. The driver-modulator interface mismatch and finite modulator bandwidth were explicitly included to reflect realistic loading conditions and bandwidth limitations.

An optimized design was developed to mitigate these impairments. Key optimization variables include the differential line width and spacing, via anti-pad geometry, ground-via shielding, return-path continuity, and driver-modulator interface matching.

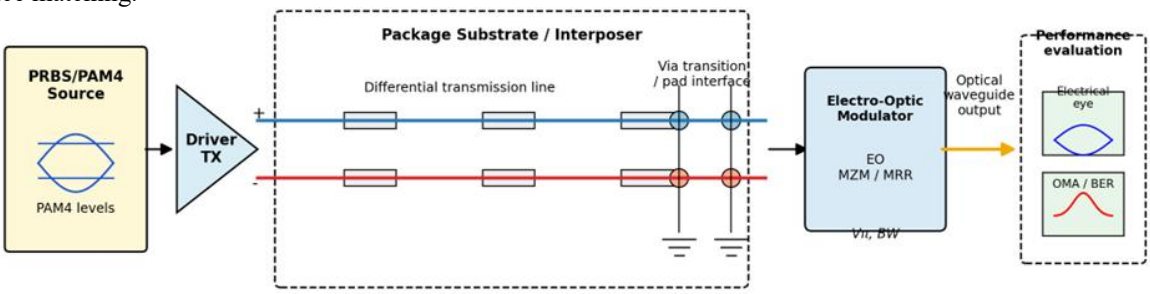

Figure 1 System-Level Simulation Setup for the Optoelectronic Integrated Interconnect

Table 1 Main Simulation Parameters

Parameter	Value
Signal format	112 Gb/s PAM4
Test pattern	PRBS13Q
Target differential impedance	100 ohm
Electrical channel length	8.2 mm
Via transitions	2
Driver output swing	1.0 Vppd
Modulator equivalent load	50 ohm ‖ 180 fF
Simulation bandwidth	0-40 GHz
Sampling points per UI	64
Evaluation metrics	S-parameters, eye diagram, BER, OMA

Figure 1 and Table 1 define the baseline model and its key configuration for the optoelectronic integrated interconnect. This baseline provides a consistent reference for comparing the electrical and optical performance of the unoptimized and optimized channel designs presented in the following subsections. The numerical results in this section represent a representative simulation scenario and should be replaced by measured or project-specific simulation data when available.

4.2 Comparison Before and After Optimization

The optimized channel was compared with the baseline design in the frequency domain to quantify the impact of the proposed improvements. The results demonstrate clear enhancements across all key electrical metrics, primarily due to restored impedance continuity, refined transitions, and reduced interconnect coupling. As shown in Figure 2 and Table 2.

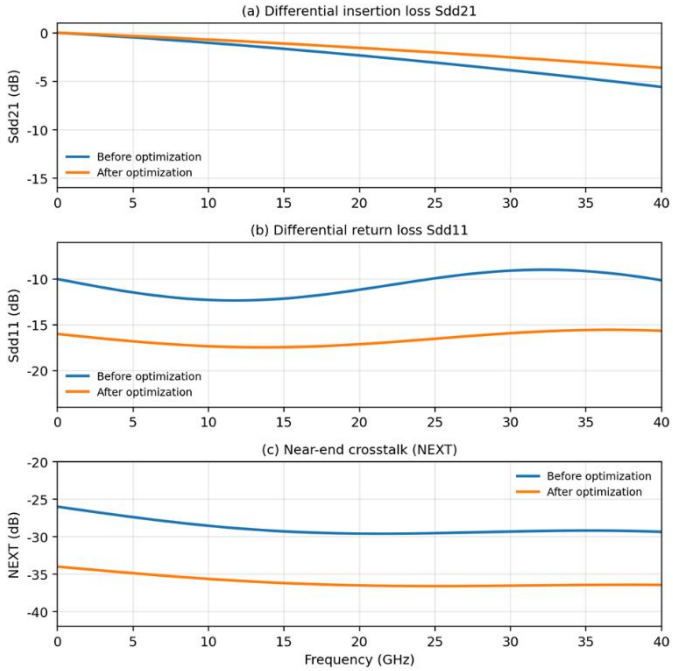

Figure 2 Frequency-Domain Comparison before and after Optimization

Table 2 Frequency-Domain Performance Comparison

Metric	Before optimization	After optimization	Improvement
Sdd21 at 28 GHz	-8.4 dB	-5.7 dB	2.7 dB lower loss
Sdd11 at 28 GHz	-11.3 dB	-17.8 dB	Better matching
NEXT at 28 GHz	-27.1 dB	-35.2 dB	8.1 dB lower crosstalk
Differential impedance variation	92-111 ohm	97-103 ohm	More stable
Estimated channel bandwidth	21.6 GHz	30.4 GHz	+40.7%
Mode conversion level	-29.4 dB	-36.8 dB	Reduced by 7.4 dB

The optimized structure substantially reduces insertion loss and improves return loss across the band. These gains are attributed to more continuous characteristic impedance along the differential path and improved return current paths through the use of denser ground-via stitching and refined transition geometries.

Furthermore, enhanced ground-via shielding and layout refinement effectively suppress inter-pair coupling. The resulting reduction in near-end crosstalk supports a higher estimated channel bandwidth and a more robust transmission environment for high-speed optoelectronic integrated interconnects. As shown in Figure 3 and Table 3.

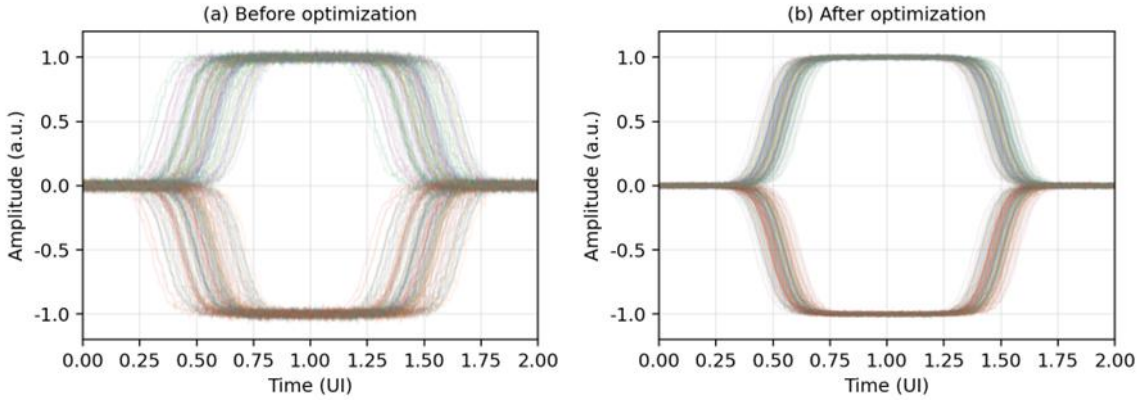

Figure 3 Representative Electrical Eye Diagram under 112Gb/sPAM4 Conditions

Table 3 System-Level Performance Comparison

Metric	Before optimization	After optimization	Improvement
Eye height	31 mV	68 mV	+119%
Eye width	0.42 UI	0.61 UI	+45.2%
RMS jitter	15.2 ps	9.1 ps	-40.1%
Optical modulation amplitude	0.41	0.63	+53.7%
Extinction ratio	3.6 dB	5.1 dB	+1.5 dB
BER	1.2 x 10^-5	2.8 x 10^-8	Strongly improved

Time-domain and system-level results further confirm the effectiveness of the proposed optimization strategy. Before optimization, the eye opening is limited and the signal transitions are more dispersed, indicating stronger ISI, reflection, and noise coupling. After optimization, the eye height increases from 31 mV to 68 mV, the eye width increases from 0.42 UI to 0.61 UI, and the RMS jitter is reduced from 15.2 ps to 9.1 ps.

More importantly, the improvement in electrical signal quality is translated into better optical modulation performance. The optical modulation amplitude increases from 0.41 to 0.63, the extinction ratio increases from 3.6 dB to 5.1 dB, and the BER is reduced from 1.2×10^{-5} to 2.8×10^{-8}. These results show that signal integrity optimization in optoelectronic integrated systems should be evaluated at both the electrical and optical levels.

4.3 Discussion on Design Trade-Offs

Although the optimization significantly improves signal integrity and modulation performance, the design must balance multiple competing objectives, including bandwidth, channel density, and power consumption. As shown in Figure 4.

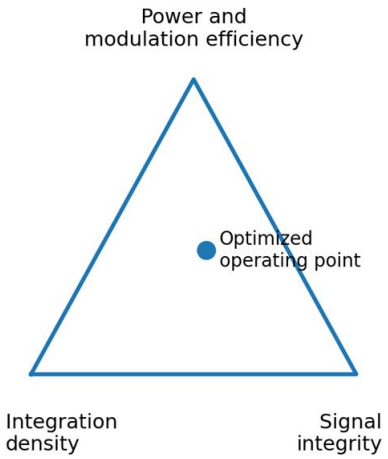

Figure 4 Main Design Trade-Offs in the Optimization of Optoelectronic Integrated Interconnects

First, wider spacing and additional shielding reduce crosstalk and improve signal integrity, but at the cost of increased routing area and lower channel density. Second, higher driver swing enhances optical modulation amplitude and link budget, yet it requires greater power consumption and places higher demands on thermal management. Third, more aggressive equalization or optimization can enhance bandwidth and reduce jitter, but may introduce additional circuit complexity and design overhead. In summary, the proposed optimization effectively improves both electrical and optical performance while maintaining a practical design balance.

5 CONCLUSION

This paper investigated the signal integrity issues and optimization design of optoelectronic integrated systems. The degradation mechanisms associated with impedance discontinuity, insertion loss, signal reflection, crosstalk, and bandwidth limitation were analyzed along the high-speed signal path, including packaging interconnects, differential transmission lines, pads, vias, and the electro-optic modulator interface. The analysis indicates that signal integrity degradation in optoelectronic integrated systems not only deteriorates the electrical eye diagram and increases the bit error rate, but also affects the effective driving voltage at the modulator input, the optical modulation amplitude, and the overall optical output quality.

To improve system transmission performance, several optimization strategies were discussed, including impedance matching and interconnect structure optimization, crosstalk suppression in high-density channels, and driver–modulator co-design. By optimizing the transmission line structure, via and pad transitions, return current paths, and electro-optic interface matching, high-frequency loss and reflection can be reduced, the eye opening can be improved, and the optical modulation performance can be enhanced. The results demonstrate that system-level optimization provides an effective link between electrical signal quality and optical output performance, offering useful guidance for the design of high-bandwidth, low-power, and highly reliable optoelectronic integrated systems.

Future work may further incorporate multi-physics simulation, thermal effect analysis, process variation modeling, and machine-learning-assisted optimization to enable more comprehensive co-design of optoelectronic integrated systems. With the continued development of silicon photonics, co-packaged optics, and three-dimensional heterogeneous integration, signal integrity optimization for higher data rates, higher channel density, and lower energy consumption will remain an important research direction.

COMPETING INTERESTS

The authors have no relevant financial or non-financial interests to disclose.

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